Abstract of the Disclosure

Disclosed is a method for translating a SPICE format circuit description to Verilog format, allowing simulation in Verilog format, or verification of prior Verilog to

5   SPICE conversion as required by some simulation programs. The invention may employ identification of SPICE sub circuits, circuit elements, input signals, and output signals; and translation of these to Verilog format wherein signal names and design hierarchy may be maintained. Instance names may be translated to Verilog names easily associated with SPICE instance names. Identification and translation may employ lookup tables,

10   rule sets, specialized field delimiters, naming conventions, other algorithms or combinations thereof. An intermediate file of input and output signals may be created. SPICE node names may be converted to Verilog wire definitions.

13